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Structural and Electrical Characterization of Si(100) Implanted with P^+ and Si^+ Ions Along the [100] Channelling Direction

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Abstract

Double implantations of 100 keV Si^+ and P^+ ions with a total dose of 1×10^{15} cm^{-2} have been performed in Si(100) along the [100] channelling direction. Buried amorphous layers of thickness 130 nm were formed beneath a crystalline top layer 60 nm thick. The phosphorus peak concentration in the buried amorphous layer varied between 2×10^{18} cm^{-3} and 6×10^{19} cm^{-3}. An enhancement of regrowth velocity by a factor of 1.2–1.45 due to phosphorus has been observed. After solid phase epitaxial regrowth of the buried layer an "interface" remains at the depth at which the two amorphous/crystalline interfaces meet. Both planar channelling analysis between the {100} planes as well as cross-sectional transmission electron microscopy show that dislocation loops are present after full recrystallization at the "buried interface". The size of the dislocation loops becomes smaller in the presence of phosphorus. The thermal stability of the buried interface during high temperature annealing depends on the size of the dislocation loops. It is largest in the absence of phosphorus. Nucleation of dislocation loops by excess phosphorus and silicon atoms occurs at the interface as shown by transmission electron microscopy. The number of phosphorus atoms involved in the nucleation of dislocation loops at the buried interface saturates at about 1×10^{14} cm^{-2}. Formation of the buried interface after recrystallization can be prevented by a successive 75 keV, 1×10^{15} Si^+ cm^{-2} random implant to amorphize the silicon top layer completely. After two-step annealing at 550 °C for 2 h then at 900 °C for 1 h the number of Hall charge carriers amounts to 90% of the implanted phorphorus dose.

1. Introduction

Channelled ion implantation has apparent advantages compared with random condition implantation. In general, a larger penetration depth results for channelled ions by which the need for high energy ion implantation may be avoided. Furthermore, damage production due to nuclear interactions is largely reduced when the ions are aligned along one of the major axes. One of the principal requirements of ion implantation is lateral uniformity over the wafer. This criterion has prevented the use of channelled ion implantation for many years.

With the recently developed medium current ion implanter at Varian/Extrion [1] one is able to perform uniform implantations under the channelling condition without ion beam shadowing effects due to the accurately parallel beam scan [2]. Recently, it has been shown that channelled ion implantation can be applied successfully with this ion implanter to obtain highly uniform doping profiles [3].

In this paper we present the structural and electrical characterization of silicon implanted with a high dose of Si^+ and P^+ ions (10^{15} cm^{-2}) along the axial [100] channelling direction. The structure obtained after implantation consists in all cases of a continuous buried amorphous layer beneath a crystalline top layer. Formation of such

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a structure was recognized previously for higher energy implantations of phosphorus into Si(111) along a random direction by Sadana *et al.* [4] and also for high dose megaelectronvolt ion implantations in silicon [5, 6].

In a recent paper we have given the preliminary results of a study on solid phase epitaxial (SPE) regrowth behaviour of buried amorphous layers formed by channelled ion implantation [7]. It was shown that the presence of phosphorus in the buried amorphous layer strongly influences the residual defect structures and their thermal stability.

In this paper we consider both the influence of phosphorus on the SPE regrowth behaviour of buried amorphous layers as well as the effect of high temperature furnace annealing (FA) and rapid thermal annealing (RTA). The buried amorphous layers were formed by double implantations of phosphorus and silicon ions in Si(100) along the [100] channelling direction. The influence of phosphorus on the SPE regrowth velocity is determined. A more detailed study than in the earlier paper [7], on the thermal stability of residual defects formed after regrowth of a buried amorphous layer, is given. The differences observed in residual defect formation after annealing of P^+ and Si^+ ion-implanted silicon are explained on the basis of a nucleation model for residual defect formation. Electrical characterization has been done by means of integral Hall measurements. It is shown that a saturation in the number of phosphorus atoms involved in the nucleation of dislocation loops occurs at the generated buried interface when the implantation dose is sufficiently high. A method to avoid nucleation of dislocation loops and to obtain a high fraction of activated dopants after annealing is presented.

2. Experimental details

Channelled implants of $^{31}P^+$ and $^{28}Si^+$ ions were performed in 125 and 150 mm, 1 Ω cm p-type CZ grown Si(100) wafers along [100]. Double implants of 100 keV P^+ and Si^+ ions were performed up to a total dose of 1×10^{15} cm^{-2}. In all cases the phosphorus ions were implanted first. Phosphorus ions were implanted with doses of 5×10^{13} cm^{-2}, 2×10^{14} cm^{-2}, 5×10^{14} cm^{-2} and 1×10^{15} cm^{-2}. In addition, silicon ions were implanted such that in all samples the total dose added up to 1×10^{15} cm^{-2}. Channelled implants were done with the Varian 220 medium current ion implanter [1]. All implants were performed at room temperature without intentional wafer cooling. The typical beam current on the target was 100 μA to avoid beam heating effects during implantation. Beam contamination due to N_2 or CO during $^{28}Si^+$ channelling ion implantation was less than 1%. This has been determined by measuring the ratios of the silicon isotopes present in the beam in comparison with the natural abundances of silicon.

Damage distributions in the as-implanted as well as in the annealed silicon have been investigated by means of Rutherford backscattering spectrometry (RBS) in combination with channelling of 1.0 and 1.4 MeV He^+ ions by using a megaelectronvolt Van de Graaff accelerator [8]. The backscattering angle was $\theta=120°$ or $\theta=170°$. Cross-sectional transmission electron microscopy (XTEM) has been performed with a Siemens Elmiskop 101 electron microscope. Samples used for XTEM investigation were thinned using both standard mechanical and ion milling procedures. The XTEM observations were done in the bright-field mode with the electron beam along [110]. Secondary ion mass spectrometry (SIMS) measurements were performed with a Cameca IMS 3f instrument to determine the phosphorus depth profiles. A primary beam of 14.5 keV, 0.1 μA Cs^+ ions was rastered over an area of 250×250 μm^2. The diameter of the area analysed was 60 μm. To avoid mass interference of ^{31}P and $^{30}Si^1H$, high mass resolution was used ($M/\Delta M=4700$). The uncertainty in the absolute depth scale was 10%.

Implanted samples were either annealed in a vacuum furnace with a base pressure of 10^{-7} Torr or by rapid thermal annealing (RTA). Furnace annealing (FA) was carried out in a standard Leybold Hereaus vacuum furnace. RTA treatments were done in an AG Associates 401 Rapid Thermal Processor under continuous argon flow. The temperature during the RTA treatment was monitored by a calibrated pyrometer and thermocouple. The maximum difference in temperature readout between thermocouple and pyrometer was approximately 20 °C at temperatures ranging from 800 to 1000 °C. The thermocouple always gave the lowest readout, mainly caused by the heat capacity of the thermocouple wires. Electrical characterization of implanted samples after thermal treatment was done by means of integral Hall measurements using a Van

der Pauw configuration [9]. A gallium/indium eutectic was used as the contact material between the external measuring probes and the sample surface to ensure ohmic contact.

3. Results

3.1. Channelled ion implantation

Buried amorphous layers were produced in Si(100) by performing double implantations of $^{31}P^+$ and $^{28}Si^+$ ions. The implantations scheme is presented in Table 1. Owing to an almost identical mass, the damage produced per incident ion is nearly the same for phosphorus and silicon ions in Si(100). Therefore the buried amorphous layers resulting from these high dose (1×10^{15} cm^{-2}) channelling implantations are nearly identical. In all cases the phosphorus ions were implanted first. Distortion of the phosphorus profile by the subsequent implantation of silicon ions is regarded to be of no importance.

The structure resulting from implantation consists of a buried amorphous layer with an average thickness of 130 nm beneath a crystalline surface layer of thickness 63.5 nm. The minimum yield in the channelling spectrum averaged 9.5%, as determined at a depth just beyond the surface peak by RBS. Although a large fraction of He^+ ions can be channelled along [100], the increase in minimum yield compared with unimplanted silicon is indicative of a large concentration of defects in the near-surface region. The RBS backscattering spectra of the as-implanted Si(100) wafers as measured along the [100] channelling direction are shown in Fig. 1. A buried amorphous layer is formed for all implantations. Only the thickness of the amorphous layer resulting from the 100 keV, 1×10^{15} P^+ cm^{-2} implantation seems to deviate somewhat from the other damage structures. A possible reason may be that the current on the target during the single phosphorus implantation was higher than for the other implantations, thereby perhaps causing heating effects [10].

A (011) cross-sectional TEM micrograph of Si(100) implanted with 100 keV, 1×10^{15} P^+ cm^{-2} along the [100] channelling direction is shown in Fig. 2. Consistent with the RBS backscattering measurement along the [100] channelling direction a buried layer can be observed of which the phase was determined to be amorphous in the (selected area) diffraction mode. The thickness of the continuous buried amorphous layer for the single phosphorus implantation, as determined by XTEM, is in close agreement with

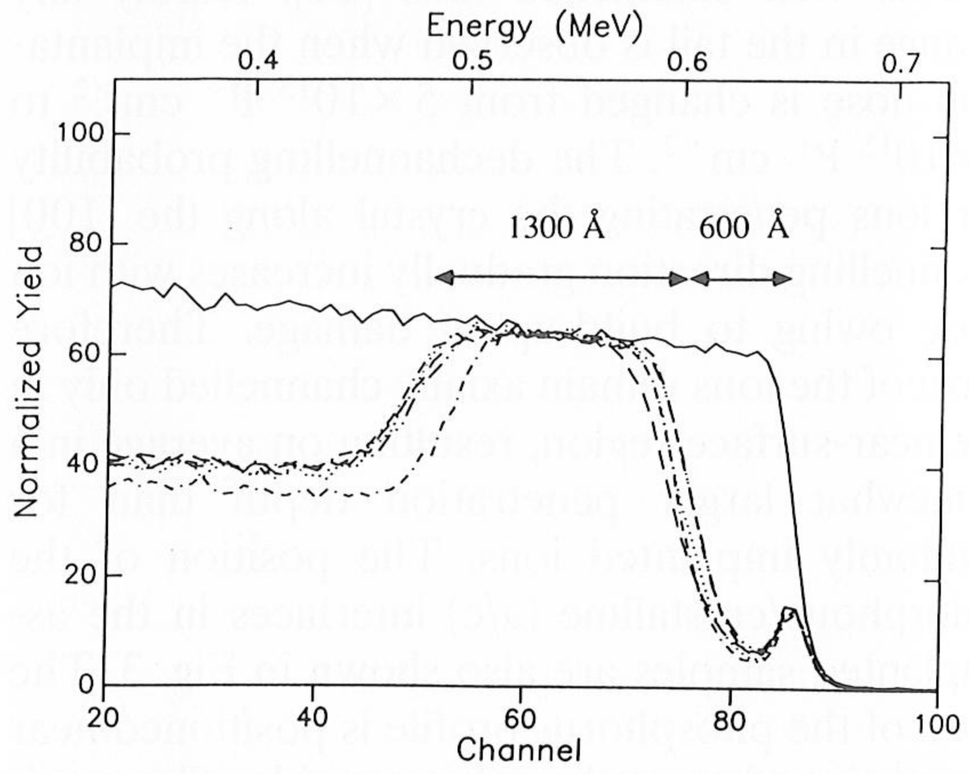

Fig. 1. Damage profiles in as-implanted silicon as measured by means of RBS in combination with channelling analysis for 100 keV dual implants of P^+ and Si^+ ions with a total dose adding up to 1×10^{15} cm^{-2}. A 1.0 MeV He^+ ion beam was used for analysis. The backscattering angle was $\theta = 170°$.

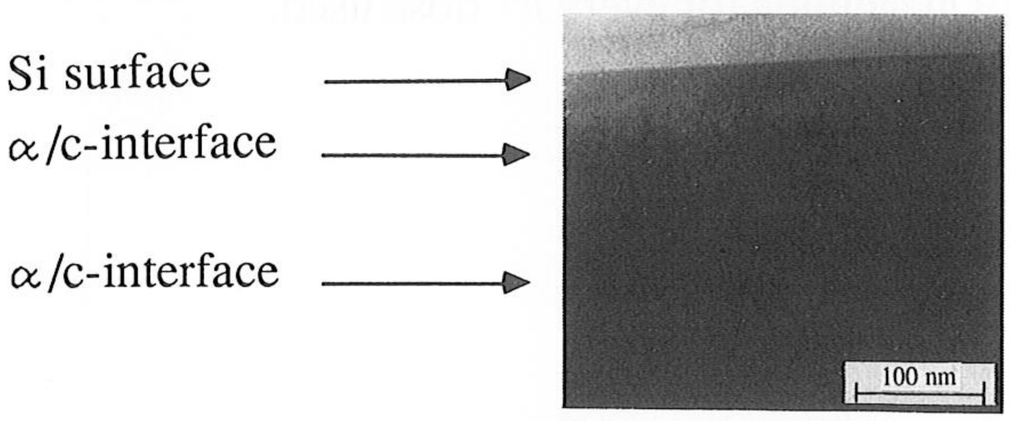

Fig. 2. XTEM micrograph along the [110] direction of silicon implanted with 100 keV, 1×10^{15} P^+ cm^{-2} along the [100] channelling direction. A buried amorphous layer of thickness 110 nm underneath a crystalline top layer of thickness 63.5 nm results.

TABLE 1 Summary of dual channelling implantations of 100 keV P^+ and Si^+ ions in c-Si(100)

Wafer number	*Implantation*
5	100 keV, 1.0×10^{15} P^+ cm^{-2}
6	100 keV, 5.0×10^{14} P^+ cm^{-2} + 5.0×10^{14} Si^+ cm^{-2}
7	100 keV, 2.0×10^{14} P^+ cm^{-2} + 8.0×10^{14} Si^+ cm^{-2}
8	100 keV, 5.0×10^{13} P^+ cm^{-2} + 9.5×10^{14} Si^+ cm^{-2}
9	100 keV, 1.0×10^{15} Si^+ cm^{-2}

the results obtained from the RBS channelling analysis at 110 nm. The micrograph shows that amorphous clusters are present in front of the buried amorphous layer at the surface side. In addition, a transition region from the amorphous to the crystalline phase about 30 nm thick is present at the substrate side.

The phosphorus profiles in the as-implanted samples were measured by means of a SIMS analysis and are shown in Fig. 3. A long tail extending to a depth of 1.0 μm is seen for all implantations considered. The tail of the implantation profile is due to well channelled ions [11]. Hardly any change in the tail is observed when the implantation dose is changed from 5×10^{13} P^+ cm^{-2} to 1×10^{15} P^+ cm^{-2}. The dechannelling probability for ions penetrating the crystal along the [100] channelling direction gradually increases with ion dose owing to build-up of damage. Therefore most of the ions remain axially channelled only in the near-surface region, resulting on average in a somewhat larger penetration depth than for randomly implanted ions. The position of the amorphous/crystalline (a/c) interfaces in the as-implanted samples are also shown in Fig. 3. The peak of the phosphorus profile is positioned near the a/c interface at the substrate side. The maximum phosphorus concentration in the buried layer was varied over nearly two orders of magnitude (2×10^{18} cm^{-3}–6×10^{19} cm^{-3}). The phosphorus concentration inside the buried amorphous layer changes over nearly one order of magnitude for every P^+ dose used.

3.2. Solid phase epitaxial regrowth of buried amorphous layers formed by channelled Si^+ and P^+ ion implantations

Solid phase epitaxial growth (SPEG) of amorphous silicon (a-Si) layers on top of a crystalline substrate has been extensively studied and reviewed [12, 13]. Here we present the results of a study on the regrowth behaviour of buried amorphous layers containing different phosphorus doping levels. During SPE regrowth the two a/c interfaces move towards each other. This is shown for silicon implanted with 100 keV, 1×10^{15} P^+ cm^{-2} along the [100] channelling direction in Fig. 4. The regrowth behaviour at 475 °C is demonstrated as a function of annealing time. After annealing for 1 h sharper transitions from the amorphous to the crystalline phase regions, compared with as-implanted silicon, result. After annealing at 475 °C for 5 h the buried layer is completely recrystallized. In the near-surface region an improved crystalline quality is obtained as can be concluded from the drop in minimum yield to 5%. The minimum yield is still higher than for unimplanted silicon showing the existence of residual defects in the near-surface region. The regrowth velocity at 475 °C was determined from the RBS channelling measurements to be 0.0023(0.0005) nm s^{-1} at the a/c interface at the surface side, in close agreement with the value of 0.002 nm s^{-1} from the literature [12]. The SPE regrowth rate at 475 °C has been determined by comparing the channel-

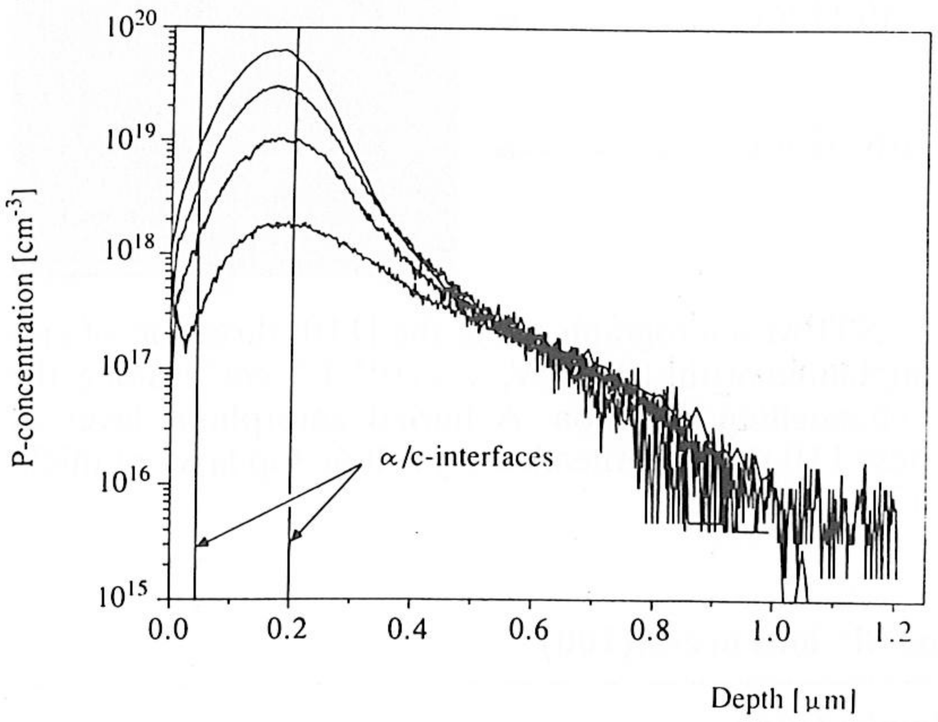

Fig. 3. SIMS profiles of silicon samples implanted with 100 keV phosphorus ions along [100] with doses of 5×10^{13} cm^{-2}, 2×10^{14} cm^{-2}, 5×10^{14} cm^{-2} and 1×10^{15} cm^{-2}. For all implantation doses a channelling tail extending to a depth of 1.0 μm is observed. The transitions from the amorphous to the crystalline phase, as measured by RBS in combination with channelling analysis, are indicated.

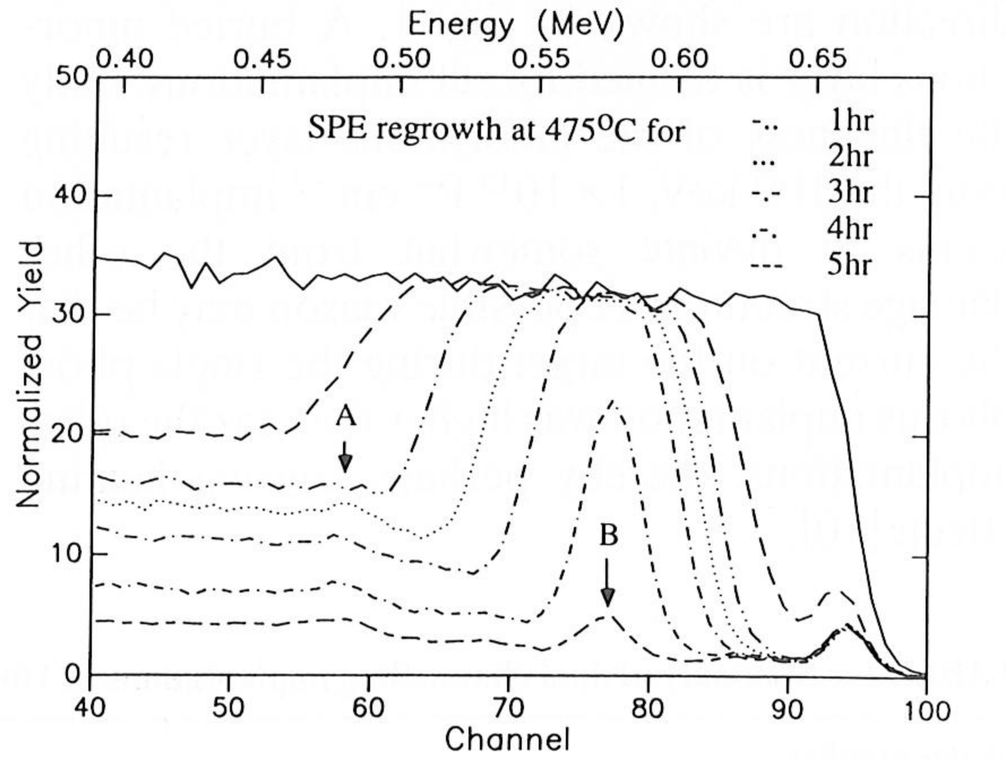

Fig. 4. SPE regrowth behaviour at 475 °C as a function of time of a buried amorphous layer formed by implantation of 100 keV, 1×10^{15} P^+ cm^{-2} in Si(100) along [100] as studied by means RBS in combination with channelling analysis. The depths at which residual type-II and -IV defects are present after annealing at 475 °C for 5 h are denoted as arrows A and B respectively.

ling spectra obtained after annealing for 1, 2 and 3 h. The regrowth velocity at the a/c interface at the substrate side is larger because of the enhancement of regrowth velocity by the presence of phosphorus. An enhancement in regrowth velocity as high as 1.45(0.20) is found for the highest phosphorus implantation dose. The enhancement of the regrowth velocity as given here represents an averaged value because the phosphorus doping level is not constant throughout the SPE regrown layer. A noticeable influence on the regrowth velocity is mentioned in the literature for volume concentrations of phosphorus above 0.08% in silicon [12, 14]. In this study the maximum volume concentration ranges from 0.004% to 0.12%.

An enhancement in the amount of dechannelling is observed in Fig. 4 at the depth corresponding to the position of the original a/c interface at the substrate side. The position where the amount of dechannelling is enhanced is shown by the arrow A in the figure. The enhancement in the amount of dechannelling can be attributed to the well-known "end of range" defects observed in ion-implanted silicon [15]. These defects are termed category II defects according to the classification scheme for ion-implantation-related defects by Jones *et al.* [16]. Moreover, at a depth of 110 nm a direct scattering contribution is observed in the RBS backscattering spectrum obtained after annealing at 475 °C for 5 h (arrow B). The position of the direct scattering peak coincides with the depth where the two moving a/c interfaces meet. Residual defects giving rise to the amount of dechannelling observed at the depth where the two moving a/c interfaces meet during regrowth are termed category IV defects [16].

The SPE regrowth behaviour has been studied for all considered implantations. In Fig. 5 RBS backscattering spectra after annealing at 550 °C for 1 h are shown. Because the regrowth velocity of amorphous silicon formed by self-implantation at this temperature is approximately 8.05 nm min^{-1} [17], annealing for 1 h ensures full recrystallization of the buried amorphous layer for all implantations. In all cases a direct scattering peak is observed in the RBS backscattering spectrum (arrow A). Figure 5 shows differences in the position of this direct scattering peak in different samples. This cannot be a consequence of the small variation in the original position of the a/c interfaces in the as-implanted silicon samples.

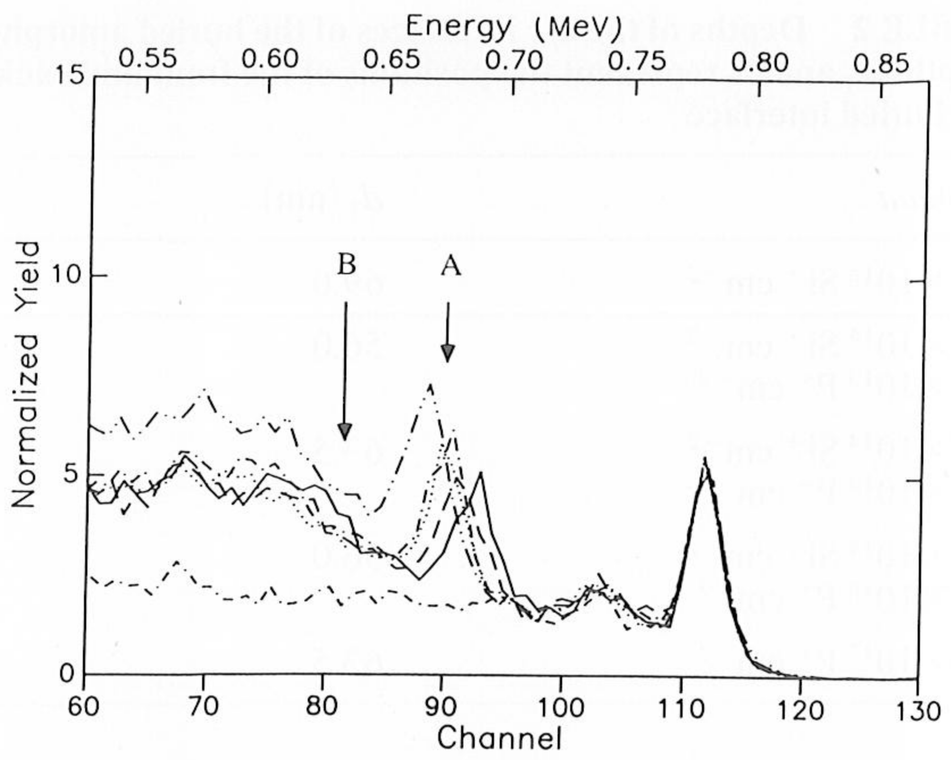

Fig. 5. Channelling spectra of double implants with 100 keV P^+ and Si^+ ions along [100] with a total dose adding up to 1×10^{15} cm^{-2} in Si(100) after SPE at 550 °C for 1 h. A direct scattering peak at the depth at which the two moving a/c interfaces meet after regrowth (arrow A) and an increase in the amount of dechannelling at the original depth of the a/c interface at the substrate side (arrow B) are observed. The direct scattering peak closest to the surface corresponds to the implantation of 100 keV, 1×10^{15} P^+ cm^{-2}. A lower phosphorus fraction of the total implantation dose results in an interface peak positioned at a greater depth below the surface.

The direct scattering peak closest to the surface corresponds to the implantation of 100 keV, 1×10^{15} P^+ cm^{-2}. A lower phosphorus fraction of the total implantation dose results in an interface peak positioned at a greater depth below the surface. The shift in position of this buried interface is related to the influence of phosphorus on the regrowth velocity; see also Fig. 3. A large gradient in phosphorus concentration exists in the buried amorphous layer, with the phosphorus concentration increasing towards the substrate side. Therefore a difference in regrowth velocity may be expected at the two a/c interfaces. An overview of the regrown layer thicknesses from the substrate and surface sides is shown in Table 2. In this table d_1 and d_3 correspond to the positions of the a/c interfaces at the front and back sides of the buried amorphous layers in the as-implanted samples. The amorphous layer thickness is equal to $d_3 - d_1$. The depth d_2 corresponds to the position of the buried interface after recrystallization. The ratio of the regrown layer thicknesses $(d_3 - d_2)$ and $(d_2 - d_1)$ is given in the fifth column. A ratio of 1.0 is expected in the case of silicon self-implantation (100 keV, 1×10^{15} Si^+ cm^{-2}). The ratio of 1.04(0.05) that has been determined for silicon self-implantation is in agreement with the

TABLE 2 Depths of the a/c interfaces of the buried amorphous layers and depth of the buried interfaces after recrystallization. Depths d_1 and d_3 represent the positions of the front and back side a/c interfaces respectively while d_2 represents the position of the buried interface

Implant	d_1 (nm)	d_2 (nm)	d_3 (nm)	$(d_3-d_2)/(d_2-d_1)$
1.0×10^{15} Si^+ cm^{-2}	69.0	131	195.5	1.04 (0.05)
9.5×10^{14} Si^+ cm^{-2} 5.0×10^{13} P^+ cm^{-2}	56.0	120	197.5	1.22 (0.07)
8.0×10^{14} Si^+ cm^{-2} 2.0×10^{14} P^+ cm^{-2}	63.5	121	196	1.31 (0.11)
5.0×10^{14} Si^+ cm^{-2} 5.0×10^{14} P^+ cm^{-2}	56.0	116.5	191.5	1.25 (0.10)
1.0×10^{15} P^+ cm^{-2}	63.5	110	177	1.45 (0.20)

TABLE 3 Summary of the contents and width of the buried interface peaks compared with the surface peak in the RBS channelling spectra

Implant	*Integral int. peak/ integral surf. peak*	$FWHM_{int.\ peak}$ (keV)	*Correction factor*	$FWHM_{int.\ peak}/FWHM_{surf.\ peak}$
1.0×10^{15} Si^+ cm^{-2}	1.06	18.3	0.80	0.97
9.5×10^{14} Si^+ cm^{-2} + 5.0×10^{13} P^+ cm^{-2}	0.94	18.0	0.81	0.97
8.0×10^{14} Si^+ cm^{-2} + 2.0×10^{14} P^+ cm^{-2}	0.85	18.7	0.81	1.01
5.0×10^{14} Si^+ cm^{-2} + 5.0×10^{14} P^+ cm^{-2}	0.79	18.2	0.82	0.99
1.0×10^{15} P^+ cm^{-2}	0.82	16.3	0.82	0.89

expected value. For all implantations involving phosphorus atoms the ratio is significantly higher than unity. This enhancement in regrowth velocity owing to the presence of phosphorus is observed for a lower volume concentration than the extrapolated value based on the experiments by Elliman *et al.* [14] and also according to the experimental data of Jeon *et al.* [18].

The amount of dechannelling as a function of depth, from the position of the buried interface towards the substrate side as observed in Fig. 5, can be decomposed into two components: a direct scattering contribution leading to the buried interface peak (arrow A) and an indirect scattering contribution causing a gradual increase in the amount of dechannelling as a function of depth (arrow B). The contents of the direct scattering peak are very similar to that of the surface peak. In Table 3 the ratio of the contents of the surface peak and the buried interface peak is given. For all implantations the ratio is close to unity, but this ratio decreases with the fraction of implanted phosphorus ions. This shows that the number of atoms at the interface "visible" to the ion beam decreases when the fraction of implanted phosphorus ions increases. The width of the buried interface peak is on average 20% larger than for the surface peak, the variation in the width of the different buried interfaces being small (10%) and not correlated with the phosphorus dose. The width of the buried interface peak is enlarged owing to energy loss straggling of the analysing megaelectronvolt He^+ ion beam. The total beam energy loss straggling along the ingoing *and* outgoing paths can be expressed in terms of the Bohr straggling [19, 20]. Calculation of the Bohr straggling along the ingoing path for normal incidence of the He^+ ions and an averaged depth of the buried interface of $z = 120$ nm gives $\Omega_B = 3.0$ keV, and therefore the total energy loss straggling as calculated along the ingoing and outgoing paths is equal to $\Omega_{tot} = 4.6$ keV and consequently the energy loss straggling amounts to $\delta E_{ES} = 10.8$ keV. Correction for the energy loss straggling of the He^+ ion beam gives $FWHM_{corr} = 0.82 \times FWHM_{meas}$ ($z = 120$ nm),

resulting in a width equal to that of the surface peak, as summarized in column 5 of Table 3. From RBS channelling analysis alone, it can be concluded that a sharp interface results with an interface roughness within the resolution of the silicon surface barrier detector ($\delta E \approx 15$ keV).

The indirect scattering contribution leading to a gradual increase in the amount of dechannelling is most obvious in the case of silicon self-implantation (100 keV, 1×10^{15} Si^+ cm^{-2}) as observed in Fig. 5 by consideration of the yield just beyond the direct scattering peak (arrow B). To investigate the residual defect structures responsible for the indirect scattering contribution, planar channelling [21] and XTEM analyses were performed. The cross-section for dechannelling of the He^+ ions channelled along the [100] direction is inversely proportional to the critical angle for channelling [22], $\sigma_d \propto 1/\psi_{1/2}$. Therefore the planar channelling analysis leads to an enhanced sensitivity for defects compared with the axial channelling analysis; see also ref. 23. The minimum yield $\chi_d(z)$ in the crystal containing residual defects can be expressed by

$$\chi_d(z) = \chi_v(z) + \{1-\chi_v(z)\} \times \left\{1-\exp\left(-\lambda_{dech}\int_0^z n(z')\,dz'\right)\right\} \quad (1)$$

where λ_{dech} denotes the dechannelling width per dislocation unit length, $\chi_v(z)$ the minimum yield in unimplanted silicon and $n(z')$ the length of dislocation lines per unit volume projected in the plane normal to the beam direction [21]. A more convenient form of expression (1) is given by

$$\ln\left(\frac{1-\chi_d(z)}{1-\chi_v(z)}\right) = \lambda_{dech}\int_0^z n(z')\,dz' \quad (2)$$

The left-hand side of eqn. (2) is called the dechannelling parameter. In the case of silicon self-implantation the depth at which $\chi_d(z)$ and $\chi_v(z)$ were determined as functions of the analysing He^+ ion beam energy was $z = 140$ nm, just beyond the position of the buried interface. Energy-dependent planar channelling analysis shows that the dechannelling parameter $-\ln\{(1-\chi_d)/(1-\chi_v)\}$ is dependent on the square root of the incident He^+ ion beam energy up to $(E)^{1/2} = 1.2$ $(MeV)^{1/2}$ for silicon self-implantation (100 keV, 1×10^{15} Si^+ cm^{-2}), as shown in Fig. 6.

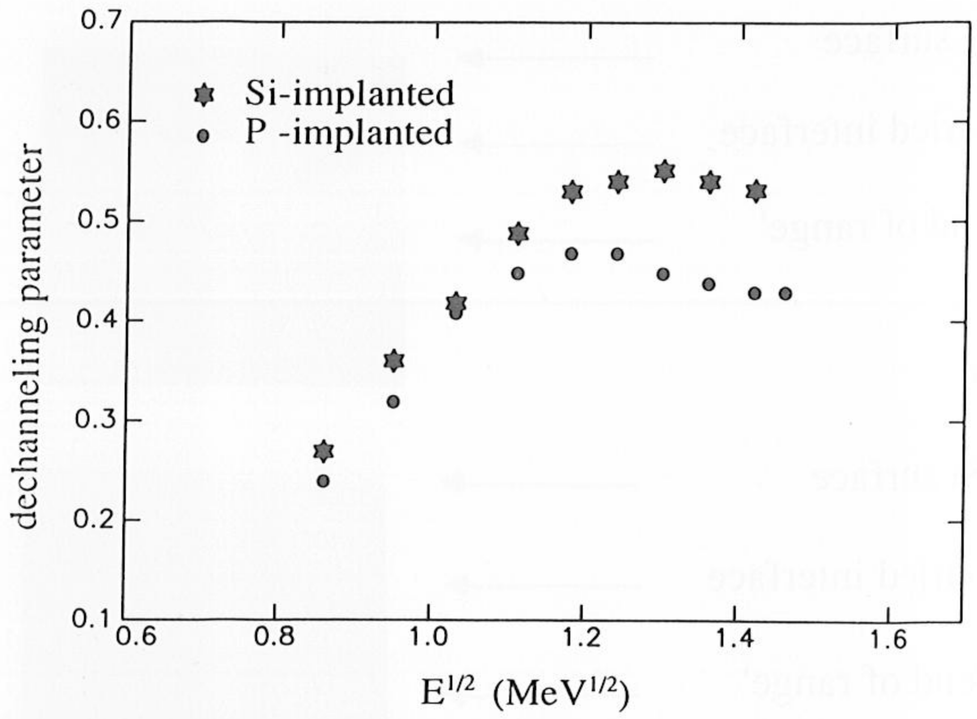

Fig. 6. Dependence of the dechannelling parameter $-\ln\{(1-\chi_d)/(1-\chi_v)\}$, as measured at a depth of $z = 140$ nm, on the energy of the incident helium ion beam for silicon implanted with 100 keV, 1×10^{15} P^+ cm^{-2} and 1×10^{15} Si^+ cm^{-2} after thermal treatment at 550 °C for 1 h.

Above $(E)^{1/2} = 1.2$ $(MeV)^{1/2}$ the dechannelling parameter levels off and is at a maximum at 1.3 $(MeV)^{1/2}$. In the case of implantation of 100 keV, 1×10^{15} P^+ cm^{-2} the dechannelling parameter has a similar energy dependence but levels off at 1.0 $(MeV)^{1/2}$ and is at a maximum at 1.2 $(MeV)^{1/2}$.

The $(E)^{1/2}$ dependence of the dechannelling parameter for both phosphorus and silicon ion implanted silicon is indicative of the presence of dislocation loops at the interface [24]. In the case of silicon self-implantation the dechannelling parameter increases linearly up to a higher energy than for the phosphorus ion implantation in silicon. This must be caused by the presence of larger dislocation loops than in the phosphorus-implanted silicon. The contribution to the amount of dechannelling from residual defects in the layer on top of the buried interface is assumed to be negligible.

Additional information about the residual defect structure remaining after full recrystallization of the buried amorphous layer has been obtained from cross-sectional TEM analysis. In Fig. 7(a) a (011) cross-sectional TEM micrograph is shown of silicon implanted along the [100] channelling direction with 100 keV, 1×10^{15} P^+ cm^{-2} after an annealing treatment at 550 °C for 1 h. In the figure the positions of the silicon surface and the buried interface as well as the position of the original a/c interface at the substrate side are indicated. At the depth corresponding to the position of the original a/c interface at the surface side a low concentration of small dislocation loops (about 10 nm in diameter) is present

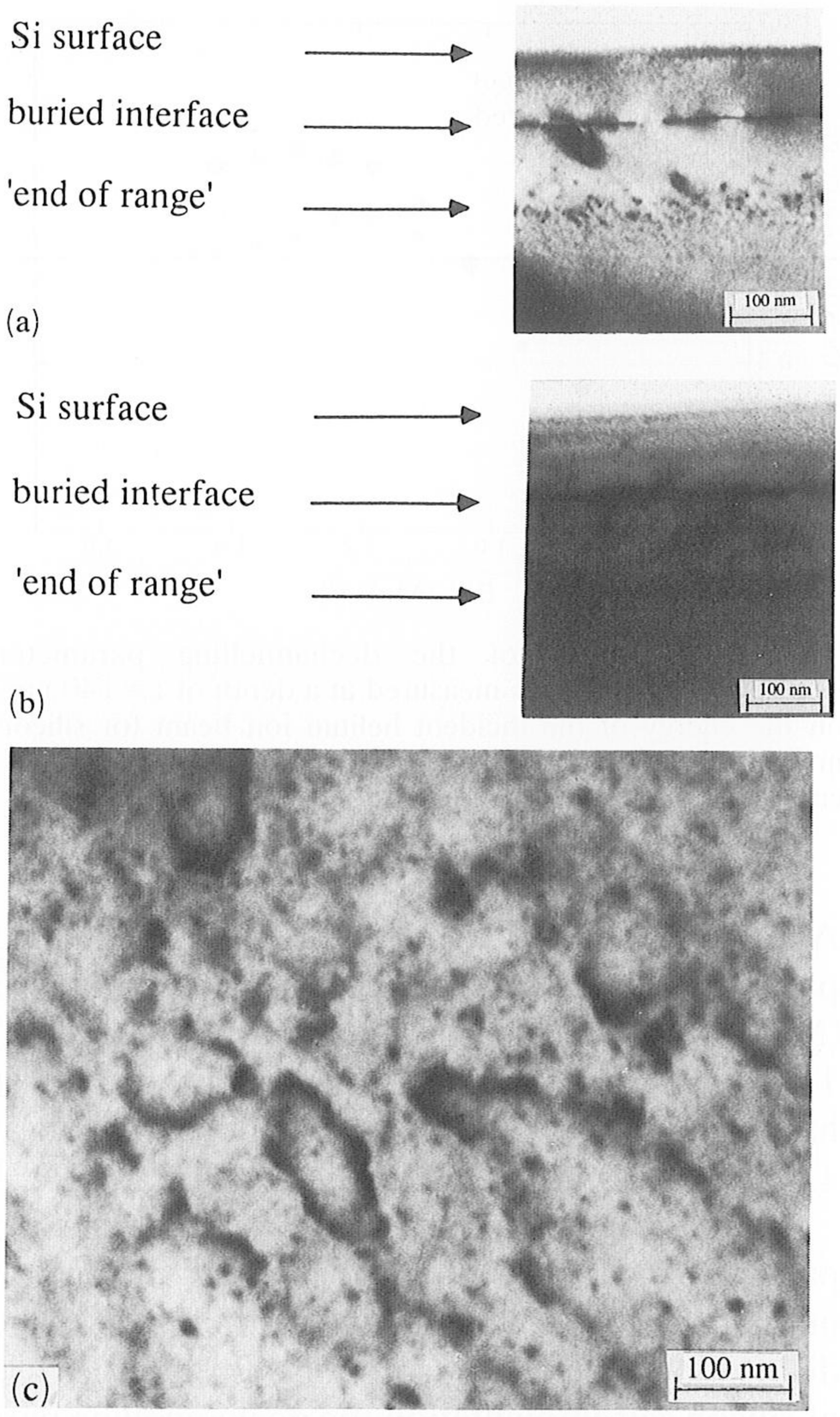

Fig. 7. XTEM micrograph of silicon implanted with (a) 100 keV, 1×10^{15} P^+ cm^{-2} and (b) 100 kV, 1×10^{15} Si^+ cm^{-2} along [100] after thermal treatment at 550 °C for 1 h. A buried interface can be observed at the depth at which the two moving a/c interfaces meet during regrowth. A band of dislocation loops is observed just beyond the depth of the original a/c interface at the substrate side and a low concentration of dislocation loops at the depth of the original a/c interface at the surface side. (c) Plan view TEM micrograph in the bright-field mode of silicon implanted with 100 keV, 1×10^{15} P^+ cm^{-2} along [100] after annealing at 550 °C for 1 h. A projection of category-II and -IV defects is shown. Category-IV defects are present at the buried interface and category-II defects arise from the "end of range" region.

after the annealing treatment at 550 °C for 1 h. These dislocation loops arise upon annealing because of the condensation of interstitials into dislocation loops in the transition region between the amorphous and crystalline phases. Additionally, a high concentration of small "end of range" [15] dislocation loops (about 10 nm in diameter) is observed just beyond the depth of the original a/c interface at the substrate side.

From channelling analysis it has been concluded that a buried interface with a roughness within the resolution of the silicon surface barrier detector used for RBS analysis exists after the recrystallization process is completed. The cross-sectional TEM image of Fig. 7(a) indeed shows the existence of a sharp interface at a depth of 110 nm. At the buried interface dislocation loops are pinned, as can be observed in Fig. 7(a). In Fig. 7(b) a (011) cross-sectional TEM micrograph is shown for a silicon sample implanted along the [100] channelling direction with 100 keV, 1×10^{15} Si^+ cm^{-2} after annealing at 550 °C for 1 h. The quality of the regrown silicon layer in between the band of "end of range" dislocation loops and the buried interface is clearly lower than in the case of the phosphorus-implanted silicon. Again, a low concentration of dislocation loops is observed in the near-surface region as well as a band of "end of range" dislocation loops near the depth of the original a/c interface at the substrate side. The size of the residual defects (dislocation loops) at the buried interface is clearly largest for the Si^+ ion implanted silicon as observed by comparison of Figs. 7(a) and (b). This is consistent with the RBS channelling measurements shown in Fig. 5.

A plan view image of a silicon sample implanted with 100 keV, 1×10^{15} P^+ cm^{-2} and annealed at 550 °C for 1 h is shown in Fig. 7(c). In this image the projection of both category IV defects at the buried interface as well as category II defects originating from the "end of range" damage are seen. The small black dots are the same as the "end of range" dislocation loops seen in Figs. 7(a) and (b). The network of larger dislocation loops is the top view of the buried interface of Fig. 7(a).

A detailed XTEM micrograph of the residual defect structures at the buried interface is shown in Fig. 8 for Si^+ ion-implanted silicon. The dislocation loops at the interface have diameters up to 30 nm. This maximum size of the dislocation loops is consistent with the value deduced from planar channelling analysis for the Si^+ ion-implanted silicon. The energy at which the dechannelling parameter has a maximum value, as shown in Fig. 6, is defined as the transition energy E_s [24]. Below this transition energy E_s, the dechannelling cross-section λ_{dech} is proportional to $(E)^{1/2}$. This energy dependence suggests that the displacement field of the dislocation loop coincides with that for a straight dislocation [25]. Above the transition energy E_s the periods of the oscillating He^+ ions between the {100} planes are much larger than the region of influence of the

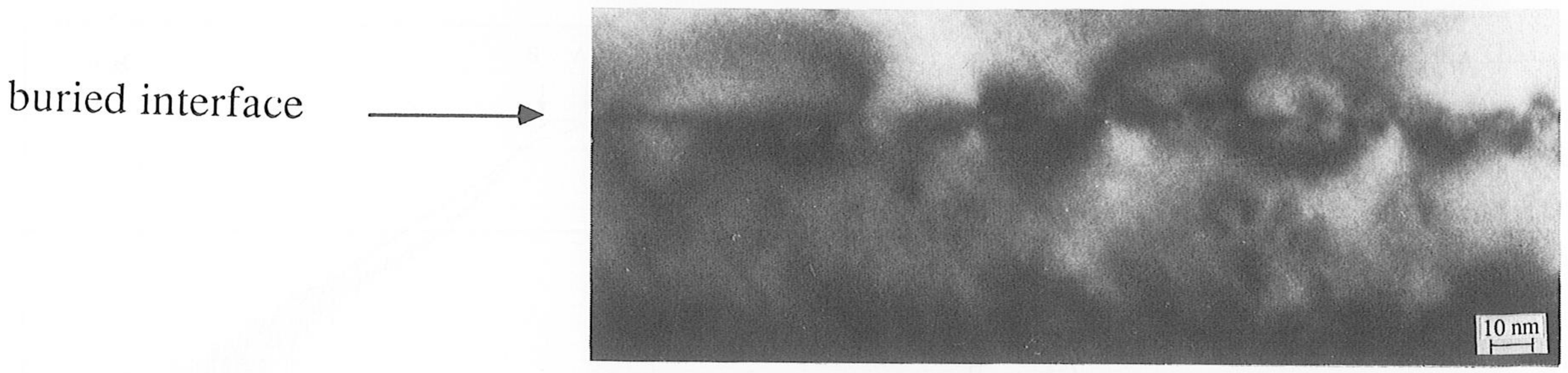

Fig. 8. XTEM micrograph of silicon implanted with 100 keV, 1×10^{15} Si^+ cm^{-2} along [100] after thermal treatment at 550 °C for 1 h, showing the buried interface in detail. A sharp buried interface is observed at which dislocation loops of maximum diameter up to about 30 nm are pinned.

dislocation loop. Therefore the dechannelling parameter becomes independent of energy above E_s. At the transition energy the wavelength of channelled He^+ ions is assumed to be comparable with the mean size of the dislocation loops present at the interface [24]. The average wavelength λ for ions between the {100} planes can be estimated from the expression given by Datz *et al.* [26]:

$$\left(\frac{\lambda}{2\pi}\right)^{-2} = \frac{a_1}{E} + \left(\frac{3b_1}{2E}\right) A^2 \qquad (3)$$

In eqn. (3) λ represents the wavelength of the oscillatory motion, E the ion energy, A the oscillation amplitude and a_1, b_1 the coefficients in the polynomial expression for the potential [26] encountered by the channelling He^+ ions:

$$V(y) = V(0) + a_1 y^2 + b_1 y^4 + \ldots \qquad (4)$$

Here, y represents the distance of the ion from the {100} plane. The potential for planar motion, using a Thomas–Fermi type of potential, can be expressed by [27]

$$V^{pl}(y) = 2\pi Z_1 Z_2 e^2 N_p \{ y^2 + 3a^2{}_{TF})^{1/2} - y \} \qquad (5)$$

The Thomas–Fermi screening radius is represented by a_{TF}; Z_1 and Z_2 are the atomic numbers of the incoming ion and target atom and N_p represents the density of atoms in the {100} atomic plane. Expansion of the potential leads to the following expression for λ:

$$\lambda = 2\pi \left\{ \frac{c_1}{(2Ec_2{}^{1/2})} + \frac{(3c_1 A^2}{(16 c_2{}^{3/2} E)} \right\}^{-1/2} \qquad (6)$$

where $c_1 = 2\pi Z_1 Z_2 e^2 N_p$ and $c_2 = 3a^2{}_{TF}$. By substitution of $E = E_s$ in eqn. (6), an estimated dislocation loop diameter of $D_{disl} \approx 30$ nm is found, in agreement with the TEM results. In the deduction of the dislocation loop diameter from the planar channelling analysis we have not taken into account the concentration or any information about the geometry of the dislocation loops. A more quantitative analysis requires information about the geometry and concentration of the dislocation loops [28].

3.3. High temperature annealing

In addition to SPE regrowth the annealing behaviour during high temperature (both FA and RTA) treatment has been studied. Prior to high temperature treatment, samples were always first SPE regrown by annealing at 550 °C for 1 h. In Figs. 9(a) and 9(b) the channelling spectra of 100 keV, 1×10^{15} Si^+ cm^{-2} and 1×10^{15} P^+ cm^{-2} implanted Si(100) are shown respectively after RTA at temperatures ranging from 800 to 1000 °C. After RTA at 800 °C for 60 s no change in the RBS backscattering spectrum of Fig. 9(a) can be observed for Si^+ ion-implanted silicon compared with the spectra after SPE (Fig. 5). After RTA at 900 °C for 60 s the direct scattering peak starts to shrink. Prolonged annealing at 900 °C leads to a further shrinkage and eventually complete disappearance ($t_{anneal} = 120$ s) of the direct scattering contribution. This is not shown here. Annealing at 1000 °C for 60 min leads to an appreciable lowering in the amount of dechannelling, as shown in Fig. 9(a). Both the amount of dechannelling due to residual damage near the buried interface as well as due to "end of range" defects at the depth of the original a/c interface at the substrate side are lowered. Prolonged annealing at 1000 °C ($t_{anneal} = 150$ s) does not lead to a further reduction in the amount of dechannelling.

In the case of phosphorus-implanted silicon the direct scattering peak has completely disap-

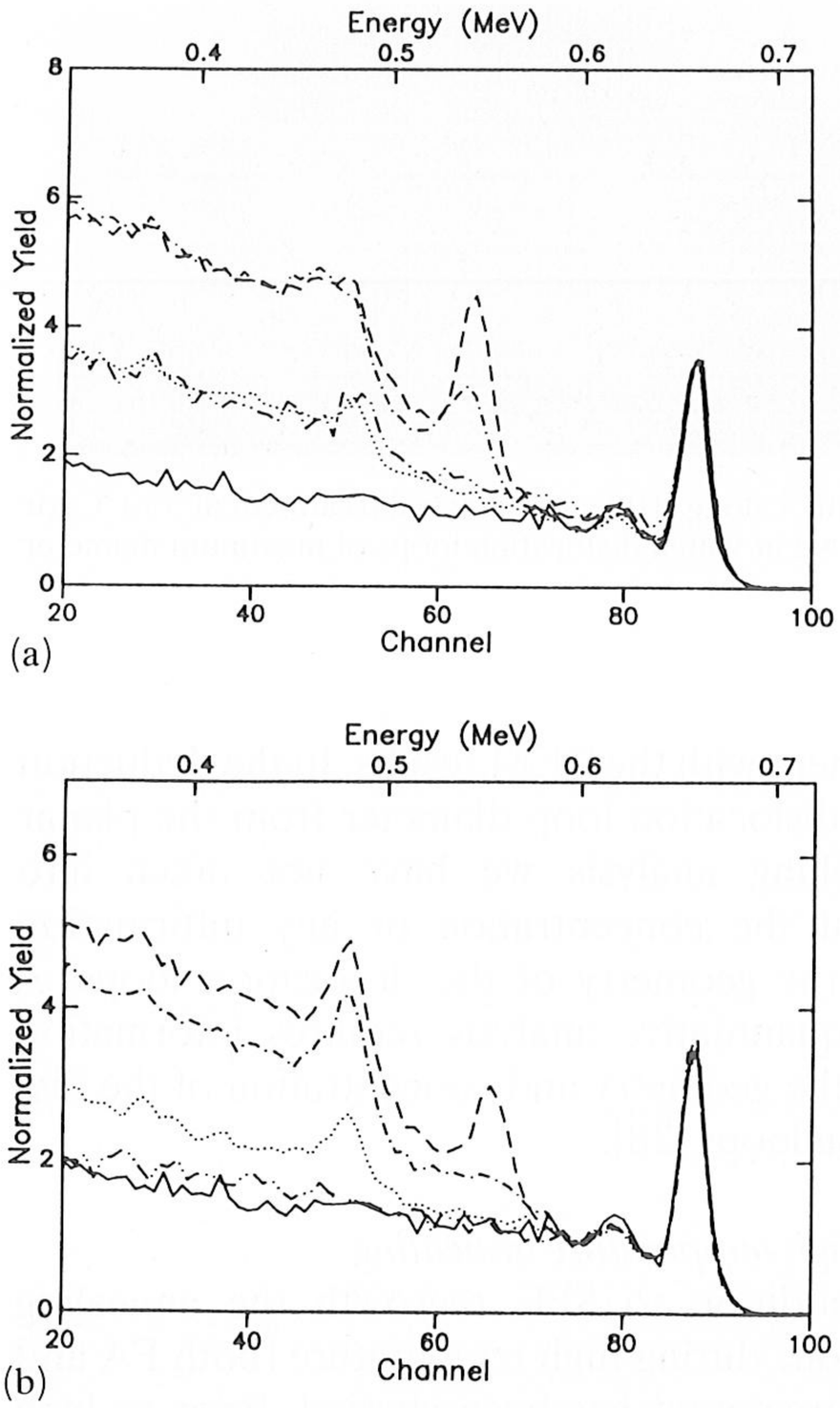

Fig. 9. Channelling spectra of silicon implanted with (a) 100 keV, 1×10^{15} Si^+ cm^{-2} and (b) 100 keV, 1×10^{15} P^+ cm^{-2} after RTA at 800 °C for 60 s (– – –), 900 °C for 60 s (– · – ·), 1000 °C for 60 s (...) and 1000 °C for 150 s (– · ·). In all cases SPE at 550 °C for 1 h was done as the first annealing step. For comparison the channelling spectrum of unimplanted silicon is also shown (——).

peared after annealing at 900 °C for 60 s; see Fig. 9(b). However, the residual amount of dechannelling due to indirect scattering processes is still clearly visible in Fig. 9(b) at the depth of the buried interface. Prolonged annealing at 900 °C ($120\,s \leqslant t_{anneal} \leqslant 240\,s$) does not lead to any further change in the RBS channelling spectrum for phosphorus-implanted silicon. After RTA at 1000 °C for 60 s no enhancement in the amount of dechannelling compared with unimplanted silicon, caused by the presence of the buried interface, can be observed. Additionally, the amount of dechannelling due to "end of range" damage shows a significant decrease. After RTA at 1000 °C for 150 s the amount of dechannelling is not significantly higher than in the case of unimplanted silicon.

The results after FA are very similar to those after RTA, although the temperature at which

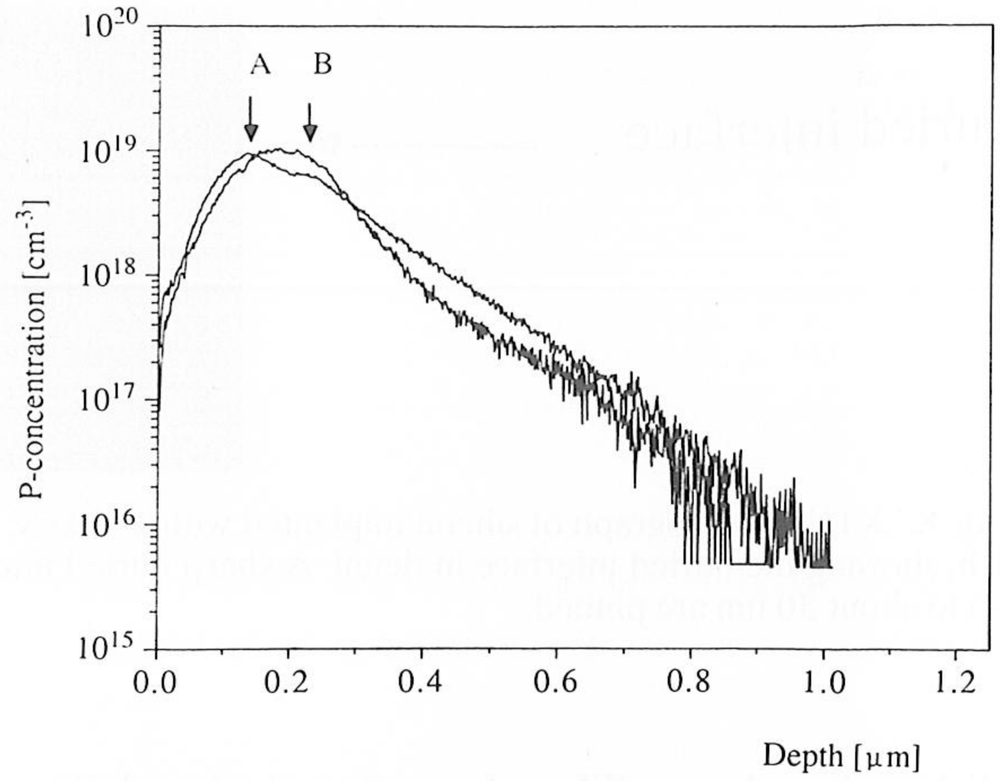

Fig. 10. SIMS profiles of silicon samples implanted with 100 keV, 2×10^{14} P^+ cm^{-2} and additionally 8×10^{14} Si^+ cm^{-2} along [100]. The phosphorus profiles of the as-implanted and annealed samples are shown. The annealing was done at 550 °C for 1 h followed by 900 °C for 1 h. In the annealed sample two peaks are observed in the phosphorus profile at depths corresponding to the positions of the buried interface (arrow A) and the "end of range" dislocation loops (arrow B).

reduction of the direct scattering peak occurs is lower. For samples implanted with silicon ions the direct scattering peak starts to shrink at a temperature of 850 °C for 30 min. Complete disappearance of the peak is only accomplished for temperatures greater than 900 °C and an annealing time of 30 min. In the case of phosphorus-implanted silicon the direct scattering peak has already completely disappeared after furnace annealing at 850 °C for 30 min.

A SIMS profile of a sample implanted with 100 keV, 2×10^{14} P^+ cm^{-2} and additionally 100 keV, 8×10^{14} Si^+ cm^{-2} along [100] is shown in Fig. 10. In addition, the phosphorus profile is shown after two-step annealing at 550 °C for 1 h followed by 900 °C for 1 h. After thermal treatment two peaks can be distinguished in the resulting phosphorus profile. Phosphorus atoms are agglomerated at the two depths at which an increase in the amount of dechannelling due to residual damage has been observed in the channelling spectra for annealed silicon. The peak closest to the surface coincides with the depth at which residual type-IV defects were observed in the XTEM micrographs of Figs. 7(a) and 7(b) (arrow A). The peak at the substrate side is positioned at the depth at which the residual "end of range" type-II defects were observed (arrow B).

The formation of category IV defects at the buried interface during annealing of a buried

amorphous layer can be avoided by amorphization of the surface region. A set of samples, containing a buried amorphous layer, has been implanted with 75 keV, 1×10^{15} Si^+ cm^{-2} to amorphize the crystalline silicon (c-Si) surface layer. The RBS and channelling spectra resulting from measurements on as-implanted and annealed samples are shown in Fig. 11. These samples were implanted with 100 keV, 1×10^{15} P^+ cm^{-2} along the [100] channelling direction prior to amorphization of the surface. The channelling spectrum of the as-implanted sample shows that a fully amorphized layer of approximate thickness 180 nm on top of a crystalline substrate is formed. After the additional implantations the samples were thermally treated in a vacuum furnace at 550 °C for 2 h to recrystallize the amorphous layer. Solid phase epitaxial regrowth is accomplished by the movement of a single a/c interface towards the surface thus preventing the formation of type-IV defects. A subsequent annealing treatment at 900 °C for 1 h was done to improve further the crystalline quality of the regrown layer and to activate the phosphorus dopants. In Fig. 11 the channelling spectrum after a two-step thermal treatment is also shown. To a depth of about 180 nm the amount of dechannelling observed in the annealed sample is identical with that in unimplanted silicon. Beyond this depth the amount of dechannelling is higher in the implanted sample. The depth at which the amount of dechannelling starts to rise more rapidly than for unimplanted silicon coincides with the depth of the "end of range" damage.

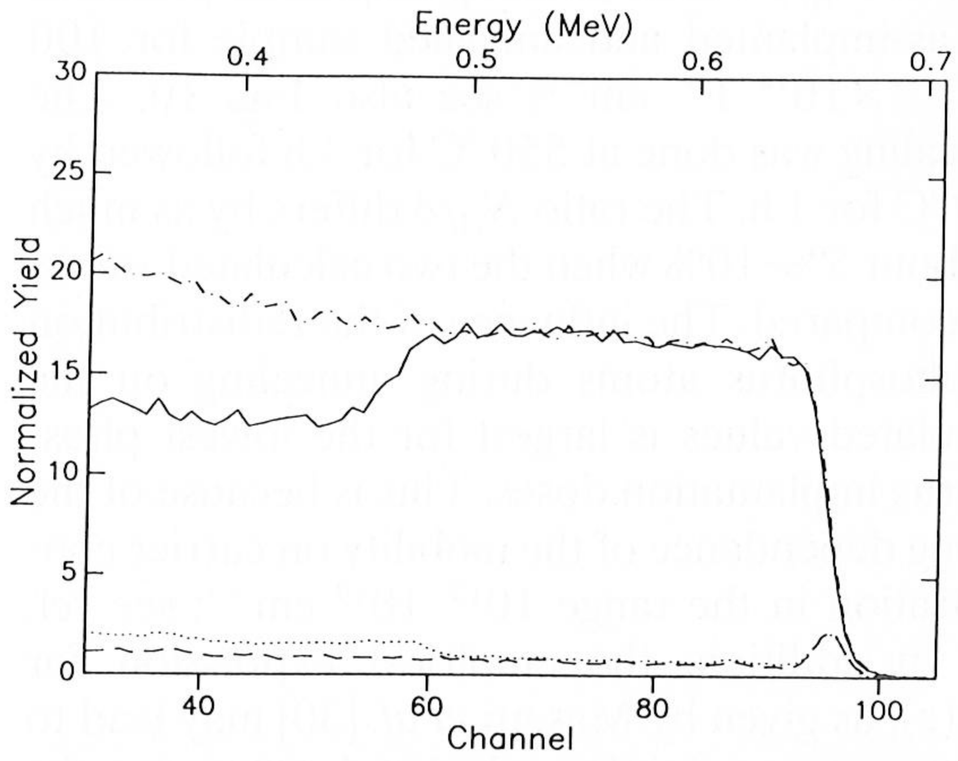

Fig. 11. Channelling spectra of silicon samples implanted with 100 keV, 1×10^{15} P^+ cm^{-2} along [100] and additionally implanted with 75 keV, 1×10^{15} Si^+ cm^{-2} along a random direction. The spectra before (——) and after (...) annealing at 550 °C for 2 h followed by annealing at 900 °C for 1 h are shown. In addition, the random (–·–) and channelling (– – –) spectra of unimplanted silicon are shown.

3.4. Electrical characterization

In addition to RBS and SIMS analysis, electrical characterization was done by means of integral Hall measurements. Measurements were done at room temperature. To perform the Hall measurements four ohmic contacts were applied at the corners of a square sample measuring 10 mm × 10 mm. The Hall coefficient $R_{H,s}$ and the sheet resistance R_s are calculated directly from the measured values of the Hall voltage and the voltage difference between two adjacent contacts when a current is flowing through the opposite contacts. From the Hall coefficient and the sheet resistivity we deduce the Hall mobility μ_H and the number of Hall charge carriers N_H [29]. The values of μ_H and N_H represent effective values.

Firstly, silicon samples containing only a buried amorphous layer were electrically characterized after RTA and FA. In Fig. 12 the ratio of the number of Hall charge carriers and the implanted phosphorus dose is given as a function of the implanted phosphorus dose for samples treated by RTA at 900 and 1000 °C. Before the RTA treatment samples were always SPE regrown at 550 °C for 1 h. The ratio N_H/ϕ depends strongly on the implanted dose ϕ. A relatively high number of Hall charge carriers is measured for the highest phosphorus dose after annealing at 900 °C. Annealing for a longer time ($t = 240$ s) or at a higher temperature

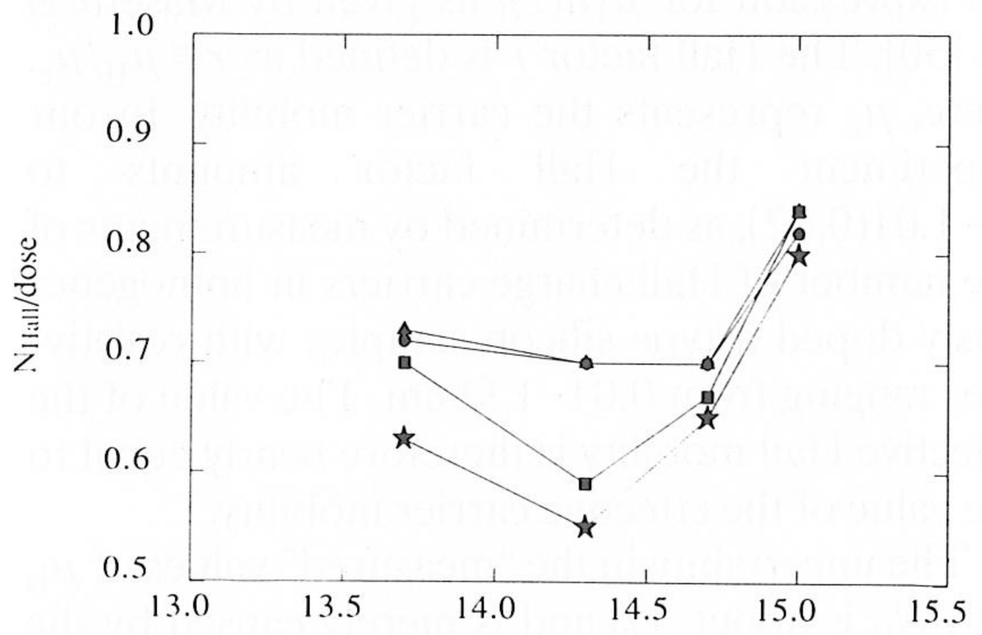

Fig. 12. Number of Hall charge carriers over implanted phosphorus dose as a function of implanted phosphorus dose after RTA at 900 °C for 60 s (★) and 240 s (■); 1000 °C for 60 s (●) and 150 s (▲). In all cases SPE at 550 °C for 1 h was performed as the first annealing step.

TABLE 4 Overview of the results of integral Hall measurements on samples treated by means of RTA at 900 °C for 60 s, 240 s and 1000 °C for 60 s, 150 s. In all cases the samples were first SPE regrown at 550 °C for 1 h

Implantation	T (°C)	t (s)	R_s (Ω/sq)	μ_H (cm² V s⁻¹)	N_H/ϕ
1×10^{15} P cm^{-2}	900	60	76 (55)	103 (116)	0.80 (0.81)
		240	82	91	0.84
5×10^{14} P cm^{-2}	900	60	124 (96)	154 (149)	0.65 (0.76)
		240	120	156	0.67
2×10^{14} P cm^{-2}	900	60	268 (177)	213 (203)	0.55 (0.75)
		240	228	234	0.59
5×10^{13} P cm^{-2}	900	60	468 (401)	425 (353)	0.63 (0.86)
		240	488	400	0.70
1×10^{15} P cm^{-2}	1000	60	66 (55)	114 (116)	0.83 (0.81)
		150	68	113	0.82
5×10^{14} P cm^{-2}	1000	60	116 (96)	152 (149)	0.71 (0.76)
		150	117	154	0.70
2×10^{14} P cm^{-2}	1000	60	251 (177)	191 (203)	0.66 (0.75)
		150	218	217	0.70
5×10^{13} P cm^{-2}	1000	60	416 (401)	416 (353)	0.73 (0.86)
		150	428	428	0.70

(T=1000 °C) leads to no significant increase in the number of measured Hall charge carriers. When a lower phosphorus dose is implanted a lower ratio of N_H/ϕ results, except for the implantation of 5×10^{13} P$^+$ cm^{-2}. The results of the electrical measurements on RTA-treated samples are summarized in Table 4. In this table the values for the sheet resistance R_s, the effective Hall mobility μ_H and the ratio of Hall charge carriers to dose N_H/ϕ, are given. The values in parentheses represent calculated values. The calculations were based on the as-implanted phosphorus profiles shown in Fig. 3. Furthermore, we assume complete electrical activation of the dopants in the calculations. The calculated values for the effective Hall mobility and the number of Hall charge carriers are obtained by using the empirical expression for $\mu\{n(z)\}$ as given by Masetti *et al.* [30]. The Hall factor r is defined as $r\equiv\mu_H/\mu_c$. Here, μ_c represents the carrier mobility. In our experiment the Hall factor amounts to r=1.01(0.02), as determined by measurements of the number of Hall charge carriers in homogeneously doped n-type silicon samples with resistivities ranging from 0.01–1 Ω cm. The value of the effective Hall mobility is therefore nearly equal to the value of the effective carrier mobility.

The uncertainty in the "measured" values of μ_H and N_H is about 5% and is merely caused by the positioning of the external point contacts. The calculated values for R_s, μ_H and N_H are based on the as-implanted phosphorus profiles. However, the annealing leads to a redistribution of the phosphorus atoms and therefore to changes compared with the tabulated values when the calculations are based on the phosphorus profiles resulting after thermal treatment. As an example, Table 5 summarizes the calculated values for R_s, μ_H and N_H/ϕ based on the phosphorus profile in the as-implanted and annealed sample for 100 keV, 2×10^{14} P$^+$ cm^{-2}; see also Fig. 10. The annealing was done at 550 °C for 1 h followed by 900 °C for 1 h. The ratio N_H/ϕ differs by as much as about 5%–10% when the two calculated values are compared. The influence of the redistribution of phosphorus atoms during annealing on the calculated values is largest for the lowest phosphorus implantation doses. This is because of the strong dependence of the mobility on carrier concentration in the range 10^{15}–10^{19} cm^{-3}; see ref. 30. In addition, the empirical expression for $\mu\{n(z)\}$ as given by Masetti *et al.* [30] may lead to an uncertainty in the calculated value for the mobility as large as 20%. This uncertainty in the calculated value for the mobility prohibits a more accurate comparison between the calculated and measured values for the effective mobility and the number of Hall charge carriers.

TABLE 5 Comparison of calculated values for R_s μ_H and N_H based on the phosphorus profile in the as-implanted and annealed sample for 100 keV, 2×10^{14} P$^+$ cm^{-2}. The annealing treatment was done at 550 °C for 1 h followed by 900 °C for 1 h

Implantation	T (°C)	R_s (Ω/sq)	μ_H (cm² V^{-1} s^{-1})	N_H/ϕ
2×10^{14} P cm^{-2}	—	177	203	0.75
	900	185	194	0.81

Table 4 shows that only for the two lowest phosphorus doses does the number of Hall charge carriers significantly increase when the annealing temperature is changed from 900 to 1000 °C.

In Fig. 13 the ratio of the number of Hall charge carriers to the implanted phosphorus dose is shown as a function of the implanted phosphorus dose for FA samples. Only for the sample implanted with a dose of 5×10^{13} P^+ cm^{-2} is a significant increase in the number of Hall charge carriers observed when the annealing temperature is increased. In Fig. 3 it was shown that the fraction of phosphorus atoms contained in the channelling tail is only significant for the lowest phosphorus implantation dose. Therefore, in the case of the lowest phosphorus dose an increase in the number of electrically active charge carriers in the tail region leads to a significant increase in the overall number of electrically active charge carriers. For all other implantation doses the number of phosphorus atoms contained in the channelling tail ($z \geqslant 0.3$ μm) is smaller than 5% of the total dose. The increase in the number of charge carriers with annealing temperature for the lowest phosphorus dose is consistent with the change in the sheet resistance, as summarized in Table 6. For the lowest phosphorus dose the sheet resistance decreases strongly when the annealing temperature is increased from 850 to 950 °C. For the higher phosphorus doses the sheet resistance remains nearly constant.

In the RBS spectra of Figs. 5 and 9 it was observed that residual type-IV defects are present at the buried interface formed after recrystallization at 550 °C for 1 h. In addition, type-II defects originating from the "end of range" damage are present near the depth corresponding to the position of the a/c interface at the substrate side. By means of channelling analysis it has also been shown that type-IV defects are avoided if the surface layer is amorphized prior to annealing; see Fig. 11. In Fig. 14 the results are shown of electrical measurements on samples which were implanted with 75 keV, 1×10^{15} Si^+ cm^{-2} in addition to the double implantation with chan-

TABLE 6 Overview of the results of integral Hall measurements on samples treated by means of FA at 850 °C for 2 h, 900 °C for 1 h and 950 °C for 30 min. In all cases the samples were first SPE regrown at 550 °C for 1 h

Implantation	*T* (°C)	R_s (Ω/sq)	μ_H ($cm^2\ V^{-1}\ s^{-1}$)	N_H/ϕ
1×10^{15} P cm^{-2}	850	67 (55)	120 (116)	0.78 (0.81)
	900	66	118	0.80
	950	66	118	0.80
5×10^{14} P cm^{-2}	850	119 (96)	160 (149)	0.66 (0.76)
	900	119	155	0.68
	950	119	154	0.68
2×10^{14} P cm^{-2}	850	229 (177)	241 (203)	0.57 (0.75)
	900	234	240	0.58
	950	220	236	0.61
5×10^{13} P cm^{-2}	850	461 (401)	440 (353)	0.62 (0.86)
	900	428	433	0.67
	950	367	405	0.84

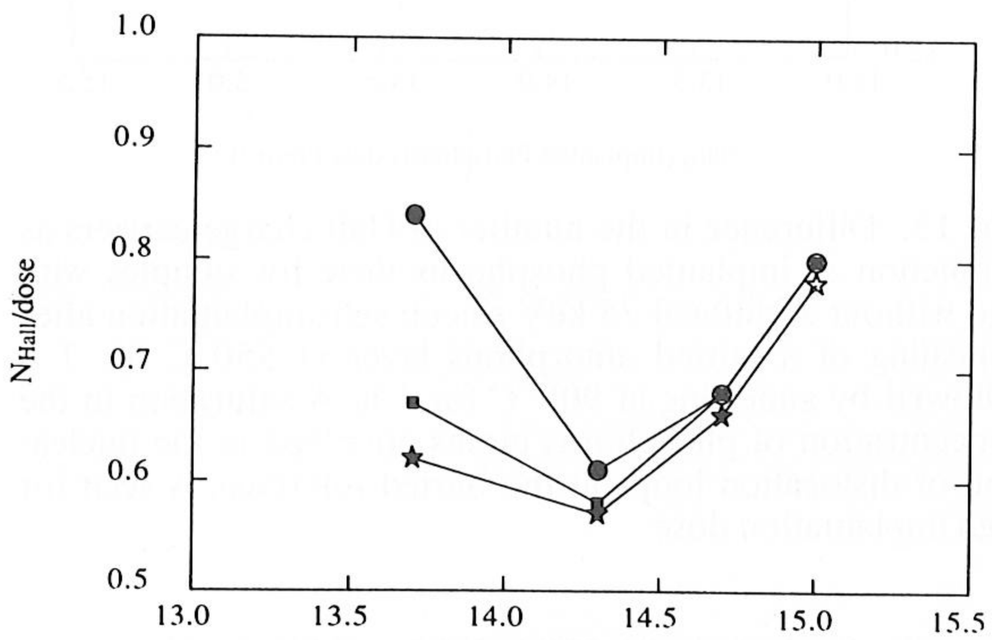

Fig. 13. Number of Hall charge carriers over implanted phosphorus dose as a function of implanted phosphorus dose after FA at 850 °C for 2 h (★), 900 °C for 1 h (■) and 950 °C for 30 min (●). In all cases SPE at 550 °C for 1 h was performed as the first annealing step. The strong dependence on annealing temperature of the lowest implantation dose (5×10^{13} P^+ cm^{-2}) is caused by activation of phosphorus in the deep channelling tail.

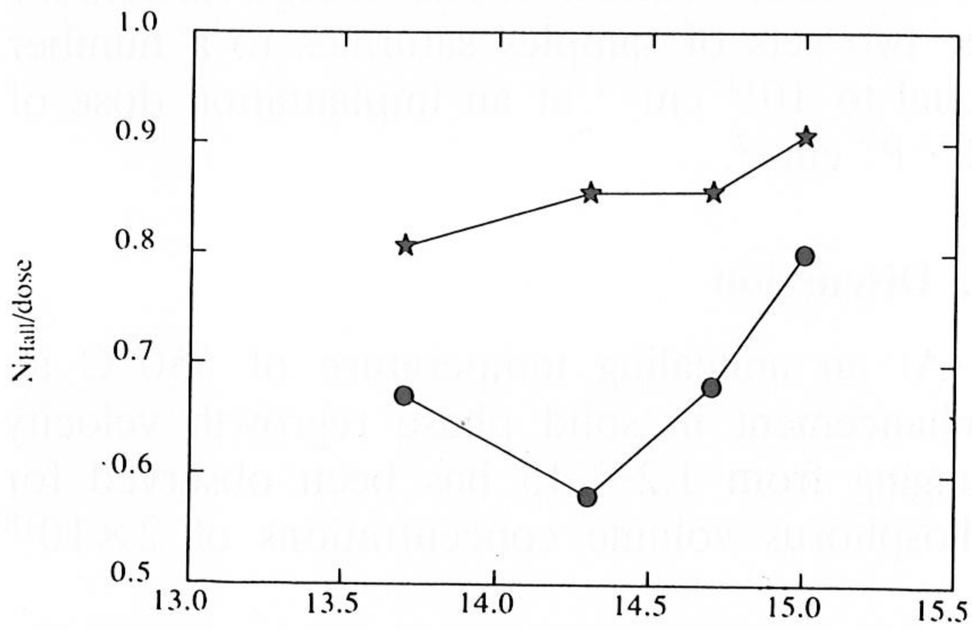

Fig. 14. Number of Hall charge carriers over implanted phosphorus dose as a function of implanted phosphorus dose of samples which were given an additional implantation of 75 keV, 1×10^{15} Si^+ cm^{-2} (★). The electrical measurements were done after two-step annealing at 550 °C for 2 h followed by annealing at 900 °C for 1 h. As a reference, the number of Hall charge carriers is shown for samples without additional silicon implantation but annealed under identical conditions (●).

nelled P^+ and Si^+ ions. Annealing treatments were done at 550 °C for 2 h followed by 900 °C for 1 h. As a reference, the results of samples of which the surface was not amorphized are also shown. A significant increase in the number of Hall charge carriers is observed for each phosphorus dose when the silicon surface is rendered amorphous by silicon self-implantation prior to the thermal treatments. In Table 7 we summarize the results for R_s, μ_H and N_H/ϕ. The sheet resistance of samples that were post-amorphized with Si^+ ions is higher than that for samples without the additional implantation: compare, for example, with the results in Table 6. The reason for this is as yet unclear.

The damage distributions in the as-implanted samples near the a/c interface at the substrate side are not affected by the additional low energy silicon self-implantation. Thus the number of phosphorus atoms involved in the formation of "end of range" dislocation loops is the same for both sets of samples. The increase in the number of Hall charge carriers must therefore be attributed to the absence of a buried interface and thus to the absence of residual type-IV defects. The number of phosphorus atoms involved in the formation of type-IV defects can be estimated by $N_P \approx N_{H,\alpha} - N_H$. Here, $N_{H,\alpha}$ and N_H represent the number of Hall charge carriers in the samples with and without the additional low energy silicon self-implantation. The difference in the number of Hall charge carriers is shown as function of the implanted phosphorus dose in Fig. 15. The difference in the number of Hall charge carriers for the two sets of samples saturates to a number equal to 10^{14} cm^{-2} at an implantation dose of 10^{15} P^+ cm^{-2}.

4. Discussion

At an annealing temperature of 550 °C an enhancement in solid phase regrowth velocity ranging from 1.2–1.45 has been observed for phosphorus volume concentrations of 2×10^{18} cm^{-3}–6×10^{19} cm^{-3} in comparison with undoped silicon. The enhancement in regrowth velocity of 1.45 for a phosphorus concentration of 6×10^{19} cm^{-3} is in good agreement with the results of Olson and Roth [13] and Elliman *et al.* [14]. The enhancement in regrowth velocity by a factor of 1.2 for a phosphorus concentration of 2×10^{18} cm^{-3} is higher than the value expected by extrapolation of experimental data for higher volume concentrations [13, 14]. In several papers the epitaxial regrowth velocity is related to the position of the Fermi level in the band gap at a moving a/c interface during recrystallization [31, 32]. The influence on the position of the Fermi level by a dopant concentration of 2×10^{18} cm^{-3} is such that the level is about 0.09 eV below the edge of the conduction band in c-Si. So, the result on the enhanced regrowth velocity for a phosphorus concentration of 2×10^{18} cm^{-3} may still support the model in which the position of the Fermi level plays an important role.

After recrystallization of a buried amorphous layer three remaining defect layers were iden-

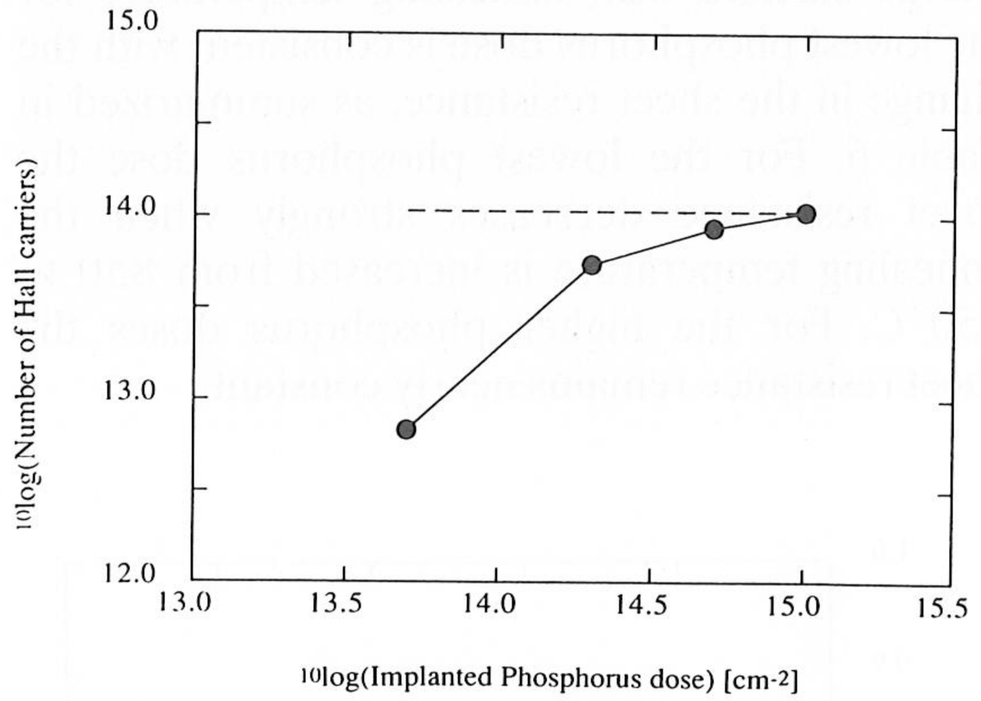

Fig. 15. Difference in the number of Hall charge carriers as a function of implanted phosphorus dose for samples with and without additional 75 keV silicon self-implantation after annealing of a buried amorphous layer at 550 °C for 1 h followed by annealing at 900 °C for 1 h. A saturation in the concentration of phosphorus atoms, involved in the nucleation of dislocation loops at the buried interface, is seen for high implantation dose.

TABLE 7 Overview of the results of integral Hall measurements on samples implanted with 100 keV P^+ and Si^+ ions in c-Si(100) under channelling conditions up to a total dose of 1×10^{15} cm^{-2} and additionally with 75 keV, 10^{15} Si^+ cm^{-2} to amorphize the silicon surface layer The samples were annealed at 550 °C for 2 h followed by 900 °C for 1 h

Implantation	T (°C)	t (s)	R_s (Ω/sq)	μ (cm^2 V^{-1} s^{-1})	N_H/ϕ
1×10^{15} P cm^{-2}	900	60	72 (55)	95 (116)	0.91 (0.81)
5×10^{14} P cm^{-2}	900	60	140 (96)	104 (149)	0.86 (0.76)
2×10^{14} P cm^{-2}	900	60	296 (177)	123 (203)	0.86 (0.75)
5×10^{13} P cm^{-2}	900	60	439 (401)	354 (353)	0.81 (0.86)

tified, irrespective of whether the buried amorphous layer was formed by silicon or phosphorus implantation. A band of "end of range" dislocation loops was observed just beyond the depth of the original a/c interface at the substrate side. Another band of dislocations with comparable size (diameter about 10 nm), but with a significantly lower density, was observed just in front of the original position of the a/c transition at the surface side. Finally, a band of dislocation loops was observed at the depth at which a buried interface formed during recrystallization. The latter defects are generally termed as category IV [16]. Category-II "end of range" dislocation loops as well as dislocation loops in the near-surface region are due to condensation of interstitial atoms and recrystallization of small amorphous zones [33]. Category-IV dislocation loops are formed because of the excess of atoms after recrystallization is completed [15].

We have observed that the dislocation loops at the buried interface are smaller in the presence of phosphorus atoms. A possible explanation for the reduction in size of the dislocation loops in the presence of phosphorus is that the nucleation of dislocation loops is enhanced by the presence of phosphorus atoms due to the generated stress field (caused by the smaller size of phosphorus atoms compared with silicon atoms incorporated in the silicon lattice [34]). The thermal stability of the buried interface has been shown to be reduced in the presence of phosphorus. The reason for the difference in stability of the interface must be related to the size of the dislocation loops which are pinned at the buried interface. The stability of the dislocation loops increases with size [15]. In the presence of phosphorus the loops are smaller hence they are less stable. A TEM study by Prussin and Jones [35] also showed that the thermal stability of dislocation loops formed in phosphorus-implanted silicon is lower than in silicon-implanted silicon.

Electrical characterization by means of integral Hall measurements showed that complete electrical activation of phosphorus atoms after high temperature treatment of silicon containing a buried amorphous layer is difficult to obtain. It was shown that a ratio of the number of Hall charge carriers and phosphorus implantation dose varying between 0.55–0.85 resulted after high temperature treatment for a phosphorus dose between 5×10^{13} cm^{-2} to 1×10^{15} cm^{-2}. The low number of Hall charge carriers is due to phosphorus atoms being associated with category-II and -IV dislocation loops. The concentration of phosphorus atoms involved in the nucleation of dislocation loops at the buried interface saturates for a high phosphorus dose (about 10^{15} cm^{-2}). The saturation is caused by a maximum in the number of dislocation loops which can be pinned at the interface.

The formation of the category-IV defects can be prevented by an additional silicon self-implantation to amorphize the silicon surface. In our case this was done by implantations of 75 keV, 1×10^{15} Si cm^{-2}. This resulted in a ratio of the number of Hall charge carriers over implanted phosphorus dose of 0.8–0.9 for an implantation dose ranging from 5×10^{13} cm^{-2}–1×10^{15} cm^{-2}. The electrical activity is still limited by the presence of residual category-II defects in the "end of range" region. Only after considerably higher annealing temperatures can this type of residual defect be annealed out [15]. Recently, Liefting *et al.* [36] have found a method to improve further the electrical characteristics of phosphorus-implanted silicon by additional megaelectronvolt silicon implantations.

We have observed in Fig. 13 a strong temperature dependence of the number of Hall charge carriers for the lowest implantation dose (5×10^{13} cm^{-2}), which is related to activation of phosphorus in the deep channelling tail. A fraction of 0.2–0.3 of implanted phosphorus atoms is contained in the deep channelling tail for an implantation dose of 5×10^{13} cm^{-2}, *i.e.* beyond the band of "end of range" dislocation loops. An annealing temperature higher than 900 °C is needed to activate fully phosphorus atoms in the channelling tail. Such a high temperature may be necessary to introduce a sufficiently high concentration of vacancies to activate phosphorus atoms. For the higher phosphorus doses this is not observed because the fraction of phosphorus in the channelling tail is less.

5. Conclusions

The regrowth behaviour of buried amorphous layers formed by channelled ion implantation of Si^+ and P^+ ions in Si(100) along the [100] direction has been studied. An SPE growth enhancement ranging from 1.2–1.45 has been found for a phosphorus dopant concentration in amorphous silicon as low as 2×10^{18} cm^{-3}–6×10^{19} cm^{-3}. After SPE regrowth a buried interface is formed

at which dislocation loops are nucleated. The nucleation of dislocation loops appears to be enhanced by the presence of phosphorus leading to dislocation loops of smaller size. The stability of the buried interface has been related to the size of the dislocation loops pinned at the interface. The stability is largest in the absence of phosphorus.

A saturation of the number of pinned phosphorus atoms at the buried interface occurs for a phosphorus dose of 1×10^{15} cm^{-2}. The maximum number of phosphorus atoms involved in the nucleation of dislocation loops at the buried interface is about 1×10^{14} cm^{-2}. The nucleation of dislocation loops at the buried interface involving phosphorus atoms can be prevented when the surface layer of the sample is amorphized by an additional silicon implantation. In this way the number of Hall charge carriers amounts to 90% of the implanted phosphorus dose.

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